Notes on SSC and Its Timing Impacts

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***ABSTRACT**: Section I explains the technique of Spread Spectrum Clocking (SSC) to reduce EMI. SSC modulation profile, modulation frequency, and modulation amount are introduced. The timing impacts of SSC on a PLL-based system are presented. The general requirements of PLL loop bandwidth frequency and phase angle of the input-to-output transfer function are also given to limit the induced PLL tracking skew.*

I. SPREAD SPECTRUM CLOCKING

Spread Spectrum Clocking (SSC) is a frequency modulation technique for EMI reduction. Instead of maintaining a constant frequency, SSC modulates the clock frequency/period along a predetermined path, i.e., the modulation profile, with a predetermined modulation frequency, f_m. Figure 1 shows a nonlinear modulation profile, known as the "Hershey Kiss" profile, patented by Lexmark International Inc. [1]. The modulation frequency is usually selected so that it is larger than 30 kHz (to be above the audio band), while small enough not to upset the host system timing. To conserve the minimum-period requirement for bus timing, the SSC clock is modulated between f_{nom} (the nominal frequency for a constant-frequency clock) and $(1- d)f_{nom}$. This is usually referred as down-spreading. $d$specifies the total amount of spreading as a relative percentage of f_{nom}.

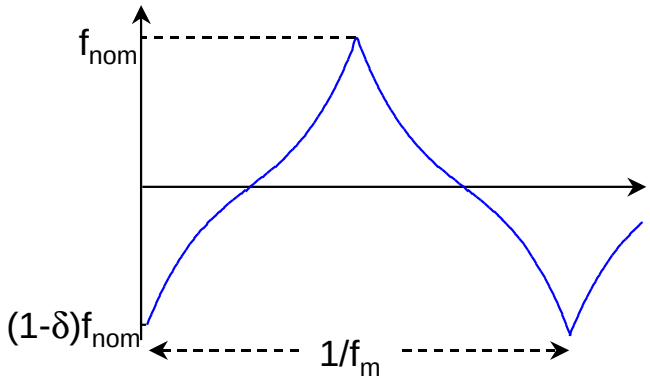


Figure 1. A typical modulation profile for SSC clocks.

The frequency modulation in the time-domain results in a frequency-domain energy redistribution of the constant-frequency clock harmonics. Figure 2 shows the spectral energy distribution of the fundamental frequency of the SSC clock in Fig.1, while the harmonic of a constant-frequency clock is also displayed for comparison. The shape of spectral energy distribution of the SSC is determined by the time-domain modulation profile, while the energy distribution width is determined by the modulation amount d The two combined determine the amount of the EMI reduction *D*. Sinusoidal modulation is usually not deployed as the modulation profile because of its uneven spectral harmonic distribution. Namely, most of the harmonic energy concentrates at the edges of the distribution, which generates much less EMI reduction capability than that of optimized nonlinear modulation profiles, e.g., "Hershey Kiss" profile. Triangle profile (linear modulation) is another form that has been used in the SSC

implementation. However, it also exibits some peaking at the edges. ***Therefore, an optimized nonlinear modulation profile maximizes the EMI reduction capability of SSC.***

The higher order harmonics have similar characteristics. The shapes of the SSC energy distribution of different harmonics are the same, and the distribution width and the amount of EMI reduction are proportional to the order of the harmonic frequency.

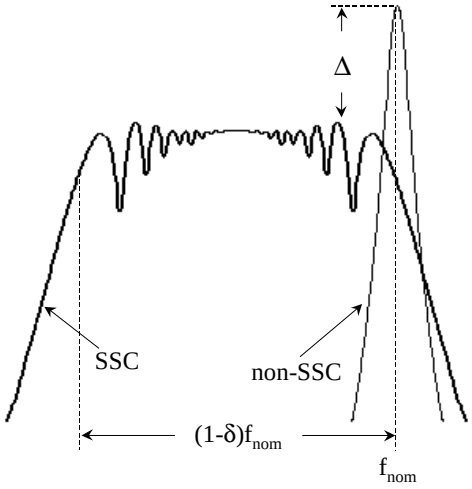


Figure 2. Spectral energy distribution of the fundamental harmonic of the SSC and non-SSC clocks.

II. SSC TIMING IMPACTS

The frequency modulation of SSC introduces certain timing impacts that are not present with constant-frequency clocks. They primarily appear in two forms: cycle-to-cycle jitter increase and downstream PLL tracking skew.

A. Cycle-to-cycle jitter increase.

To minimize timing impact, the amount of modulation is normally very small (d< 1%). The period difference between the maximum frequency and minimum frequency in a SSC clock is

$$\Delta T_{total} = \frac{1}{(1-d) f_{nom}} - \frac{1}{f_{nom}} \approx \frac{d}{f_{nom}}. \quad (1)$$

The number of clock cycles that exist in the time interval that the SSC clock migrates from f_{nom} to $(1-d)f_{nom}$ can be found as

$$N = \frac{f_{avg}}{2 f_m} = (1-0.5\,d)\frac{f_{nom}}{2 f_m}, \quad (2)$$

where f_{avg} is the average frequency of the SSC clock. In the case of linear modulation, the period slew rate is a constant. Combining Eqs. (1) and (2), the cycle-to-cycle period change, i.e., the cycle-to-cycle jitter increase due to SSC, can be expressed as

$$\Delta T_{c-c} = \frac{\Delta T_{total}}{N} = \frac{2\,d}{1-0.5\,d} \cdot \frac{f_m}{f_{nom}^2}\,. \tag{3}$$

For 100-MHz SSC clocks with 0.5% modulation and 30-kHz modulation frequency, the cycle-to-cycle jitter increase is,

$$\Delta T_{c-c} = \frac{2 \cdot 0.5\%}{1-0.5 \cdot 0.5\%} \cdot \frac{30 \cdot 10^3}{(100 \cdot 10^6)^2} = 0.03 \text{ ps}\,. \tag{4}$$

Similarly, for 66-MHz SSC clocks with 0.5% modulation and 30-kHz modulation frequency, the cycle-to-cycle jitter increase is,

$$\Delta T_{c-c} = \frac{2 \cdot 0.5\%}{1-0.5 \cdot 0.5\%} \cdot \frac{30 \cdot 10^3}{(66 \cdot 10^6)^2} = 0.07 \text{ ps}\,. \tag{5}$$

Even considering the nonlinear "Hershey Kiss" modulation profile, the cycle-to-cycle jitter increase is less than 1 ps when $d < 1\%$ and $f_m < 50$ kHz. ***Therefore, SSC has negligible cycle-to-cycle jitter increase. I.e., SSC clocks should have the same cycle-to-cycle jitter performance as their non-SSC counterparts, if SSC is implemented correctly.*** Actual measurements have verified this conclusion in practical applications.

B. Downstream PLL tracking skew.

In a PLL-based system, the downstream PLLs have limited feedback loop bandwidth. Figure 3 shows the block diagram of a PLL. As the input clock being modulated, a PLL cannot instantaneously update the output clock. The result is a slight difference between the periods of the PLL input clock and its output clock. As the input SSC clock migrates from f_{nom} to $(1-d)f_{nom}$ or the reverse, the accumulation of the period difference can result in a significant amount of phase error between the PLL input clock and the output clock [2]. This phase error is defined as the PLL tracking skew. ***This tracking skew will decrease the setup/hold margins at the corresponding interfaces.***

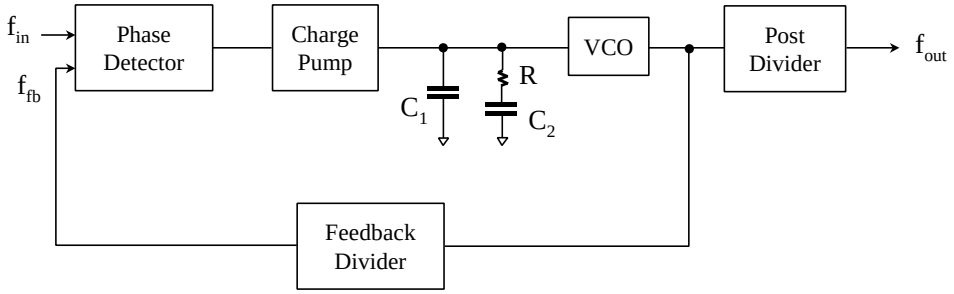


Figure 3. Block diagram of downstream PLL.

SSC modulation profiles, except sinusoidal modulation, contain higher-order harmonic contents other than that of the fundamental modulation frequency. The maximum frequency change happens when the modulation changes the polarity of its slew rate at the corners (refer to Fig. 1). In order to accurately track the sudden change of the input frequency, a PLL needs to have a sufficiently large loop bandwidth to track all the essential modulation harmonics. The loop gain of the above the PLL with a second-order low-pass filter is

$$T(s) = \frac{I_{CP}}{s} \cdot \left(\frac{1}{sC_1} \cdot \frac{s + \frac{1}{R \cdot C_2}}{s + \frac{C_1 + C_2}{R \cdot C_1 \cdot C_2}} \right) \cdot G_{VCO} \cdot \frac{1}{N_{FB}}, \tag{6}$$

where I_{CP} is the charge pump current, G_{VCO} is the VCO gain, and N_{FB} is the feedback divider. Given the parameters of a PLL, its loop bandwidth, f_B, can be determined numerically by solving the equation $|T(f_B)| = 1$.

On the other hand, the modulation frequency is typically small when compared to bus clocks. The period difference between input and output clock will be accumulated in the long modulation period. In addition to the requirement of having a large loop bandwidth to minimize the phase error, it is desirable to have a small phase angle, q, which is defined as the phase angle of the input-to-output transfer function $H(s)$ at the modulation frequency. $H(s)$ can be expressed as

$$H(s) = \frac{I_{CP} \cdot G_{VCO}}{N_{FB} \cdot C_1} \cdot \frac{s + \frac{1}{R \cdot C_2}}{s^3 + s^2 \cdot \frac{C_1 + C_2}{R \cdot C_1 \cdot C_2} + s \cdot \frac{I_{CP} \cdot G_{VCO}}{N_{FB} \cdot C_1} + \frac{I_{CP} \cdot G_{VCO}}{N_{FB} \cdot R \cdot C_1 \cdot C_2}}. \tag{7}$$

The phase angle, q, can be determined numerically as the angle of $H(s)$ at the modulation frequency, i.e., the angle of the complex number $H(j \cdot 2pf_m)$:

$$q = f\left(H(j \cdot 2pf_m)\right), \tag{8}$$

where j is the complex suffix.

III. Simulations of PLL Tracking Skews

With a complete set of the PLL parameters, which includes I_{CP}, G_{VCO}, R, C_1, C_2, and N_{FB}, the tracking performance of the PLL can be simulated. Figures 4(a)-4(d) show the simulated PLL tracking performance of three different designs of a PLL. The SSC modulation used is a "Hershey Kiss" profile with f_m = 31.5 kHz and d= 0.5%.

Figure 4(a) shows that the modulation profile can be preserved at the output clock as long as the loop bandwidth, f_B, is at least one order of magnitude higher than the modulation frequency, f_m. Figures 4(b)-4(d) show the effects of f_B and q on the tracking skew. At the moment that the slew rate of the clock period changes polarity (at the modulation corners,) it induces a sudden jump in the skew. This is because the PLL feedback loop cannot update the output clock

fast enough due to the limited bandwidth. By comparing Figs. 4(b) and 4(c) it is evident that higher f_B can significantly reduce the amount of tracking skew. The sudden jump is still present with the higher f_B, but the amplitude is much reduced.

After the initial skew jump, the feedback loop attempts to correct the frequency difference between the input clock and the output clock. So the skew starts to decrease. However, the input frequency is continuously being modulated, but at a slower skew rate (predominantly at the modulation frequency). So the tracking skew will decrease due to the combined effects of the feedback loop trying to catch up and the input clock drifting away. This low frequency effect is predominantly determined by the phase angle q. Comparing Figs. 4(c) and 4(d) shows that the PLL design with a smaller q will have less tracking skew, even when its bandwidth, f_B, is kept at the same value. ***Therefore, to minimize PLL tracking skew the PLL design needs to maximize its feedback loop bandwidth and minimize the phase angle of its input-to-output transfer function at the modulation frequency.***

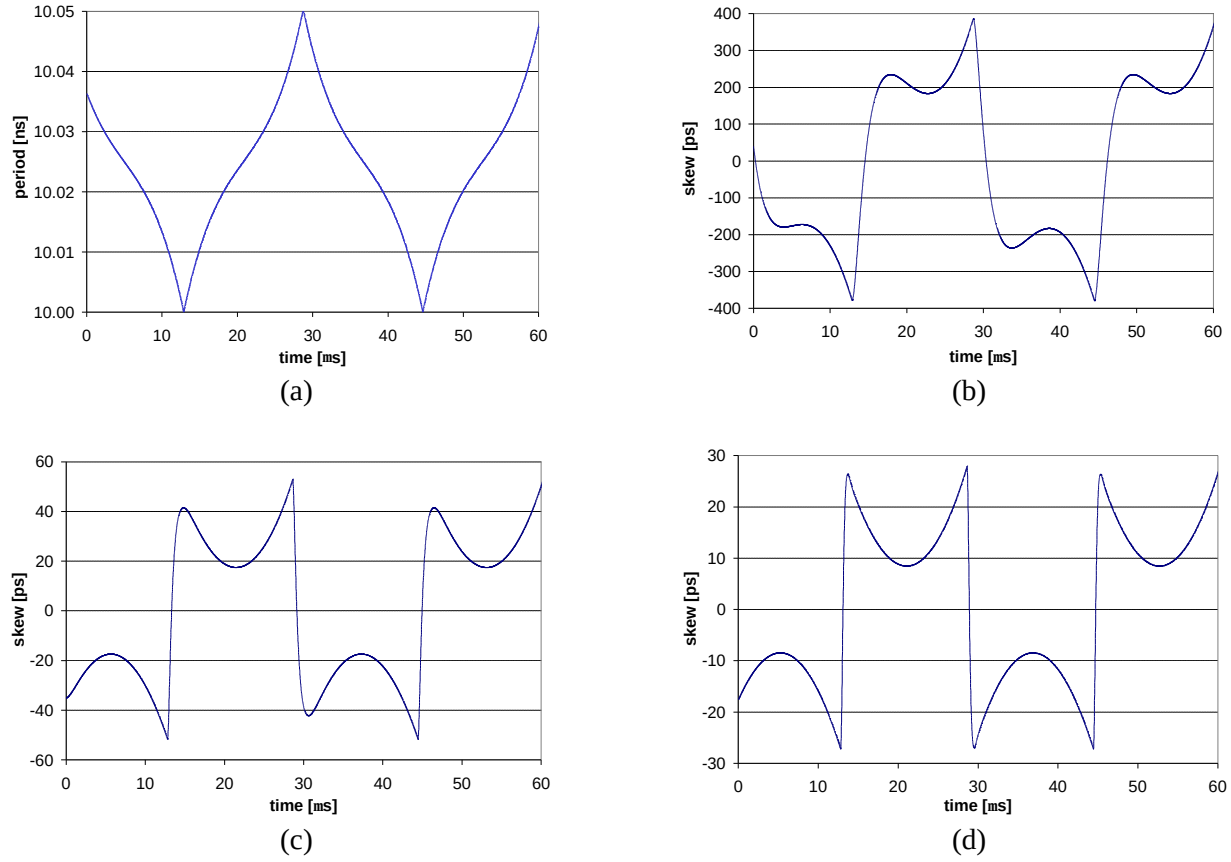
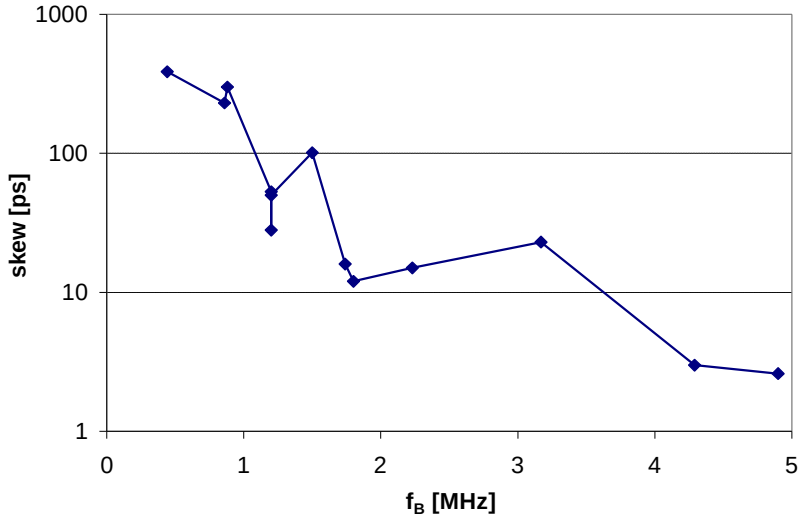


Figure 4. Simulated PLL tracking performance: (a) modulation of output clock period; (b) tracking skew for f_B = 440 kHz and q = -0.89º; (c) tracking skew for f_B = 1.2 MHz and q = -0.031º; (d) tracking skew for f_B = 1.2 MHz and q = -0.0068º.

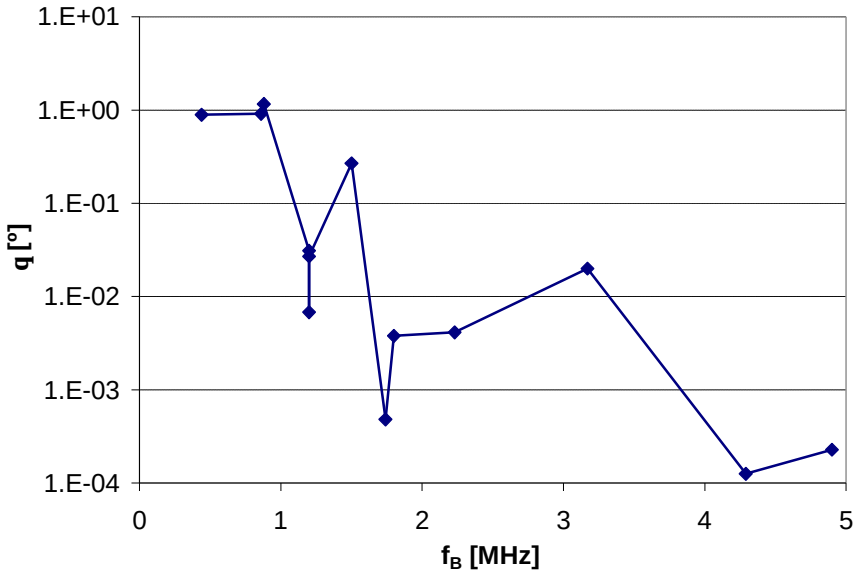
Figure 5(a) shows the PLL tracking skew as a function of the loop bandwidth, f_B. Generally PLL skew is reduced with an increase of f_B. These results are based on a 30-kHz

"Hershey Kiss" modulation profile with d = 0.5%. PLL tracking skew is proportional to d Therefore, skew numbers with different $d$values can be determined accordingly.

Generally a higher bandwidth reduces the PLL tracking skew. Some of the data points in Fig. 5(a) show otherwise. The reason is that those corresponding PLL designs have larger values of q, which are plotted in Fig. 5(b). Figures 5(a) and 5(b) provide the approximate PLL design requirements for f_B and q to limit its tracking skew. For example, in order to have less than 100-ps PLL tracking skew, the PLL needs to have f_B > 1 MHz and $|q|$ < 0.1° according to Figs. 5(a) and 5(b). To obtain the exact PLL tracking performance, simulations with specific PLL parameters are necessary.



(a)



(b)

Figure 5. PLL tracking skew as a function of f_B and q.

Compared to "Hershey Kiss" modulation, linear modulation has smaller frequency-change slew rate for the same modulation frequency and spread amount. ***So, it generally induces less skew at the expense of providing less EMI reduction capability.*** To illustrate this, Fig. 6 shows a comparison of the tracking skews of a 1.5-MHz PLL with these two modulation profiles.

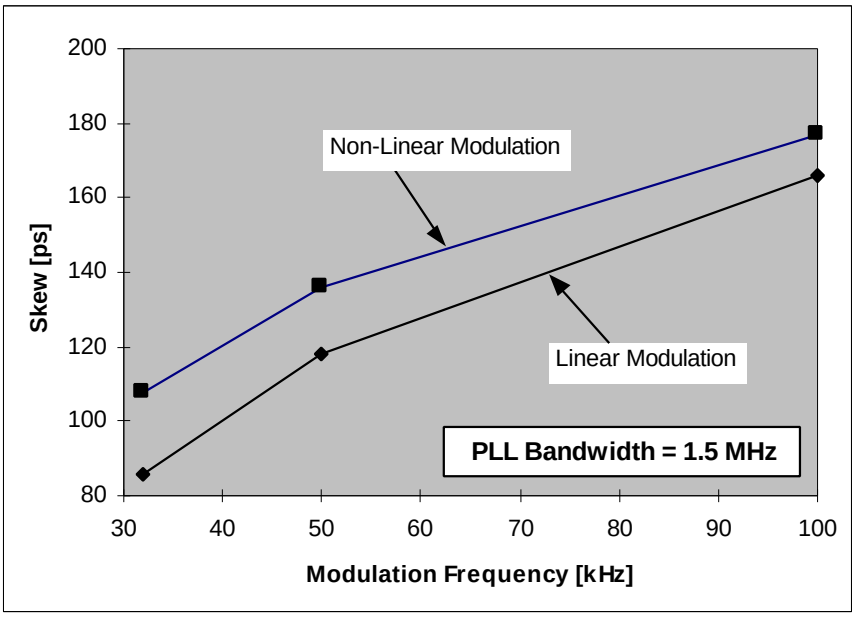


Figure 6. The PLL tracking skew comparison for a PLL with loop bandwidth of 1.5 MHz (δ = 0.5%).

IV. Design Example

Even an optimized PLL design will still have certain PLL tracking skew. This skew needs to be absorbed by existing system timing margin or compensated for by layout adjustment [3]. The following example illustrates the design considerations of an AGP-1x plug-in card. In an architecture that AGPCLK drives a PLL, and the PLL provides timing to all of chip, the system must absorb the impact of skew [3]. The designed PLL's loop bandwidth is 1.2 MHz, and the phase angle is -0.031º. The corresponding PLL tracking skew between AGPCLK and the PLL output clock is +/-130 ps. The motherboard trace length guidelines must be adjusted to compensate for the skew impact if there is no system margin for it. The needed trace length adjustment can be determined by:

$$L_{SSC} = L_{AGP} - \frac{\Delta T_{SSC}}{t_p}, \tag{9}$$

where L_{SSC} is the adjusted trace length including SSC impacts, L_{AGP} is the original AGP layout guideline, DT_{SSC} is the amount of violation of the component timing spec, and t_p is the propagation delay [3]. Using DT_{SSC} = 130 ps (assuming there is no system timing margin), the maximum motherboard line length guideline needs to be shrunk by 0.7 inch for 2:1 space routing

(no impact on the 1:1 space routing). The minimum motherboard line length guideline needs to be increased by 1.2 inch for both 2:1 and 1:1 space routing (see detail in [3]). This shrinks the AGP trace length solution space by total of 1.9 inch and 1.2 inch for 2:1 and 1:1 space routing correspondingly. ***Restricting the trace length to this reduced solution space would ensure system timing compatibility with SSC.*** Smaller skew resulting from an improved PLL design would reduce amount of the SSC impact on the solution space.

V. SUMMARY

When implementing SSC, it is important to consider its timing impacts to ensure host system compatibility. There is negligible cycle-to-cycle jitter increase (< 1 ps) when d< 1% and f_m > 30 kHz. For a PLL-based system, it is desirable to have high feedback loop bandwidth and small phase angle of the input-to-output transfer function at the modulation frequency.

Clock manufacturers need to comply with SSC specs to deliver SSC clock drivers [4]. Any PLL-based component would be required to have properly designed PLL to minimize the tracking skew. For system integrators to ensure system compatibility, system timing need to have enough setup/hold margins to absorb the induced PLL tracking skew. Otherwise, layout design must be adjusted to compensate for it.

References:

[1] K.B. Hardin, et al., "*Spread spectrum clock generation and associated metho*d," US Patent 5,488,627, January 30, 1996.

[2] K.B. Hardin, et al., "Design considerations of phase-locked loop systems for spread spectrum clock generation compatibility," *Proceedings of IEEE International Symposium on Electromagnetic Compatibility*, Aug. 1997, pp. 302-307.

[3] A. Volk, H. Heck, "*Notes on AGP interface architectures and motherboard design with SSC*," Revision 1.0, February, 1998.

[4] "*Preliminary specifications of spread spectrum clocking (SSC),*" Revision 0.2, January, 1998.